PVP 20

Code: 20EC6501

III B.Tech - I Semester – Regular Examinations - DECEMBER 2022

DIGITAL ELECTRONICS DESIGN WITH VHDL

(HONORS in ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Explain AND, OR, NOT & NAND gates using VHDL program.	L2	CO1	7 M
	b)	Analyze composite types with neat examples of digital state machine.	L4	CO2	7 M
OR					
2	a)	Explain constant declarations and signal declarations.	L2	CO1	7 M
	b)	Analyze 4-bit subtractor using VHDL code.	L4	CO2	7 M
UNIT-II					
3	a)	Explain variable and signal assignment statements with an example each.	L2	CO1	7 M
	b)	Design 2 to 4 decoder and model using VHDL.	L3	CO3	7 M
OR					

4	a)	Explain signal drivers with suitable VHDL example programs.	L3	CO1	7 M
	b)	Model VHDL code for 4:1 multiplexer.	L3	CO3	7 M
		UNIT-III			
5	a)	Model reminder calculator for any four different integers using VHDL function.	L3	CO1	7 M
	b)	Using VHDL function, model the area of circle with an example.	L3	CO3	7 M
		OR			
6	a)	Using VHDL function model binary to integer converter for simulation.	L3	CO1	7 M
	b)	Using a VHDL function model mean calculator for simulation.	L3	CO3	7 M
		UNIT-IV			
7	a)	Design a Mod 16 synchronous up counter and model using behavioural VHDL modelling.	L3	CO1	7 M
	b)	Model VHDL code and draw synthesized circuit for case statement.	L3	CO3	7 M
		OR			
8	a)	Model JK Flip-flop using behavioural VHDL modelling.	L3	CO1	7 M
	b)	Design state machine for odd parity detector of a serial line.	L3	CO3	7 M

UNIT-V					
9	a)	Design and Analyse architecture of CLB in FPGA.	L3	CO1	7 M
	b)	Implement the circuit for Half adder using PAL.	L3	CO4	7 M
OR					
10	a)	Design and model 2:1 Mux using FPGA.	L3	CO1	7 M
	b)	Explain XILINX 4000 series FPGA.	L2	CO4	7 M